(ENGLISH TRANSLATION)

OFFICIAL LETTER

Date of Receipt: August 20, 2004

FROM: The Intellectual Property Bureau
Ministry of Economic Affairs
TO: FASL LLC
C/O: Patrick I. C. Yun/William W. L. Chen,
patent attorney

SUBJECT

The rejection of patent application no. 92125514 has been tentatively concluded. Before any formal issuance of a first Office Action, the applicant is invited to submit, in duplicate, a responsive explanation (along with any amendment) and relevant rebuttal evidence within sixty (60) days of the day following the date of receipt of this Official Letter. **The deadline cannot be extended.** Failure to comply with the requirement, or a late reply to this Letter, will result in the rejection of this application.

CONTENTS

Any supplementation and/or amendment directed to this application should be conducted in accordance with the provisions in Articles 48 and 49 of the Patent Law and Article 28 of the Enforcement Rules of the Patent Law.

The applicant may request a personal interview or demonstration with the Examiner in the Response. If deemed necessary, the time and venue for holding the interview will be arranged.

The Examiner is of the opinion that:

1. There 28 claims in this application, in which claims 1 and 13 are independent claims and the rest are dependent claims.

2. The subject matter claimed in claim 1 is directed to a semiconductor device which is characterized by comprising a gate electrode formed on a gate insulation film on the semiconductor substrate, the gate electrode comprising a first polycrystalline silicon film and a second polycrystalline silicon film formed above the first polycrystalline silicon film, the second polycrystalline film being in a different crystal state from the first polycrystalline film, and at least an upper layer of the second polycrystalline silicon film being silicidized. It is noted that claim 1 of R.O.C. patent publication no. 432509 (see attachment) entitled, "A gate conductive layer provided on a semiconductor chip," which was published May 1, 2001, discloses a gate conductive layer formed on a gate oxidation layer on a silicon substrate, the gate conductive layer similarly comprising a first polycrystalline silicon film and a second polycrystalline silicon film disposed above the first polycrystalline silicon film, a silicide layer being formed above the second polycrystalline silicon film, and the crystal dimension of the second polycrystalline silicon film being different from the first polycrystalline silicon film. The semiconductor device claimed in claim 1 can be easily achieved by those of ordinary skill in the technical field of this invention based on technology in existence prior to the filing date, and cannot be deemed to involve step and, hence, failed to fulfill the provision in Article 22.4 of the Patent Law.

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3. Claim 13 discloses a method for manufacturing a semiconductor device. The main technical feature of the method has been disclosed in the cited reference (see attachment). The method for manufacturing a semiconductor device of claim 13 can be easily achieved by those of ordinary skill in the technical field of this invention based on technology in existence prior to the filing date, and cannot be deemed to involve step and, hence, failed to fulfill the provision in Article 22.4 of the Patent Law.

4. On the other hand, the "separation layer" (in claims 2 and 14), the "varying ... in crystal face orientation" (in claims 3, 4, 5, 6, 15, 16, 17 and 18) and the "smaller crystal particle diameter" (in claims 9, 10, 21 and 22) disclosed in the dependent claims can effectively control the silicidizing reaction in the second polysilicon film so as to form silicide layer of excellent quality. The "separation layer" recited in the dependent claims should be incorporated into the relevant independent claims, and the "different crystal state" recited in the independent claims should be precisely designated, so as to be distinguishable from the claimed scope of the cited reference (see attachment).

(*Translator's note:* This last paragraph is not translated herein as it only relates to the formality requirements for any documents to be submitted.)

Sealed By

The Intellectual Property Office
Ministry of Economic Affairs

經濟部智慧財產局專利申請案核駁理由先行通知書

受文者：飛索股份有限公司（代理人：惲軼群 先生、陳文郎 先生）

地　　址：臺北市松山區南京東路三段二四八號七樓

發文日期：中華民國九十三年八月十八日

發文文號：（九三）智專二（一一）04140字第〇九三二〇七七二七一〇號

主旨：第〇九二一一二五五一四號專利申請案經審查後發現尚有如說明三所述不明確之處，台端（貴司）若有具體反證資料或說明，請於文到次日起六十日內提出申復說明及有關反證資料一式二。若屆期未依通知內容辦理者，專利專責機關得依現有資料續行審查，請　查照。

說明：

一、本案如有補充、修正，應依專利法第四十八條、第四十九條、專利法施行細則第二十八條之規辦理。

二、若希望來局當面示範或說明，請於申復說明書內註明「申請面詢」，並繳交規費新台幣一千元，本局認為有必要時，另安排地點、時間舉辦「面詢」。

三、本案經審查認為：

（一）本案申請專利範圍共28項，其中第1、13項為獨立項，其餘為附屬項。

（二）請求項第1項之申請標的為一種半導體元件，其特徵為其包含一在半導體基板上之閘極絕緣膜上，形成之一閘極電極，該閘極電極包含有一第一多晶矽膜，及形成在該第一多晶膜上方之一第二多晶矽膜，該第二多晶矽膜之晶體狀態不同於該第一多晶膜，且該第二晶矽膜之至少一上層係形成為矽化物；經查九十年五月一日公告之我國專利公告編號四二五〇九，名稱為「一種設於一半導體晶片之閘極導電層」專利案（如附件）其申請專利範圍第1項即已揭露一種在矽基底上之閘氧化層上，形成一閘極導電層，該閘極導電層亦包含有一第一多晶矽層，及設於該第一多晶矽層之上方之一第二多晶矽層，且該第二多晶矽層之上方亦形成有一矽化物層，而該第二多晶矽層之晶粒尺寸不同於該第一多晶矽層，本案請求項第1項所請之半導體元件係為發明所屬技術領域中具通常知識者依申請前之先前技術所能輕易完成者，難謂具進步性，不符專利法第二十二條第四項之規定。

（三）請求項第13項則揭露一種製造一半導體元件的方法，該方法主要技術特徵亦於引證案如附件）中已揭示，請求項第13項製造半導體元件的方法係為發明所屬技術領域中具常知識者依申請前之先前技術所能輕易完成者，難謂具進步性，不符專利法第二十二條第四項之規定。

（四）惟本案於各附屬項中所揭露之「分離層」（第2、14項），「相異之晶面取向」（第3、4、5、6、15、16、17、18項），「較小的第二多晶矽膜的矽晶粒直徑」（第9、10、21、22項）可有效控制在第二多晶矽膜中的矽化反應，以形成良好品質的矽化物層；本案應將附屬項中之「分離層」併入其依附之獨立項，並將獨立項中之「晶體狀態不同」予以明確指定，以與前述引證案（如附件）之所請專利範圍有所區隔。

四、如有補充、修正說明書或圖式、圖說或圖面者，應具備補充、修正申請書一式二份，並檢送補充、修正部分劃線之說明書、圖說修正頁一式二份及補充、修正後無劃線之說明書或圖式替換頁一式三份或全份圖說一式三份；如補充、修正後致原說明書或圖式頁數不連續者，應檢附補充、修正後之全份說明書或圖式一式三份或僅補充、修正圖面者，應檢附補充修正後全份圖面一式三份至局。